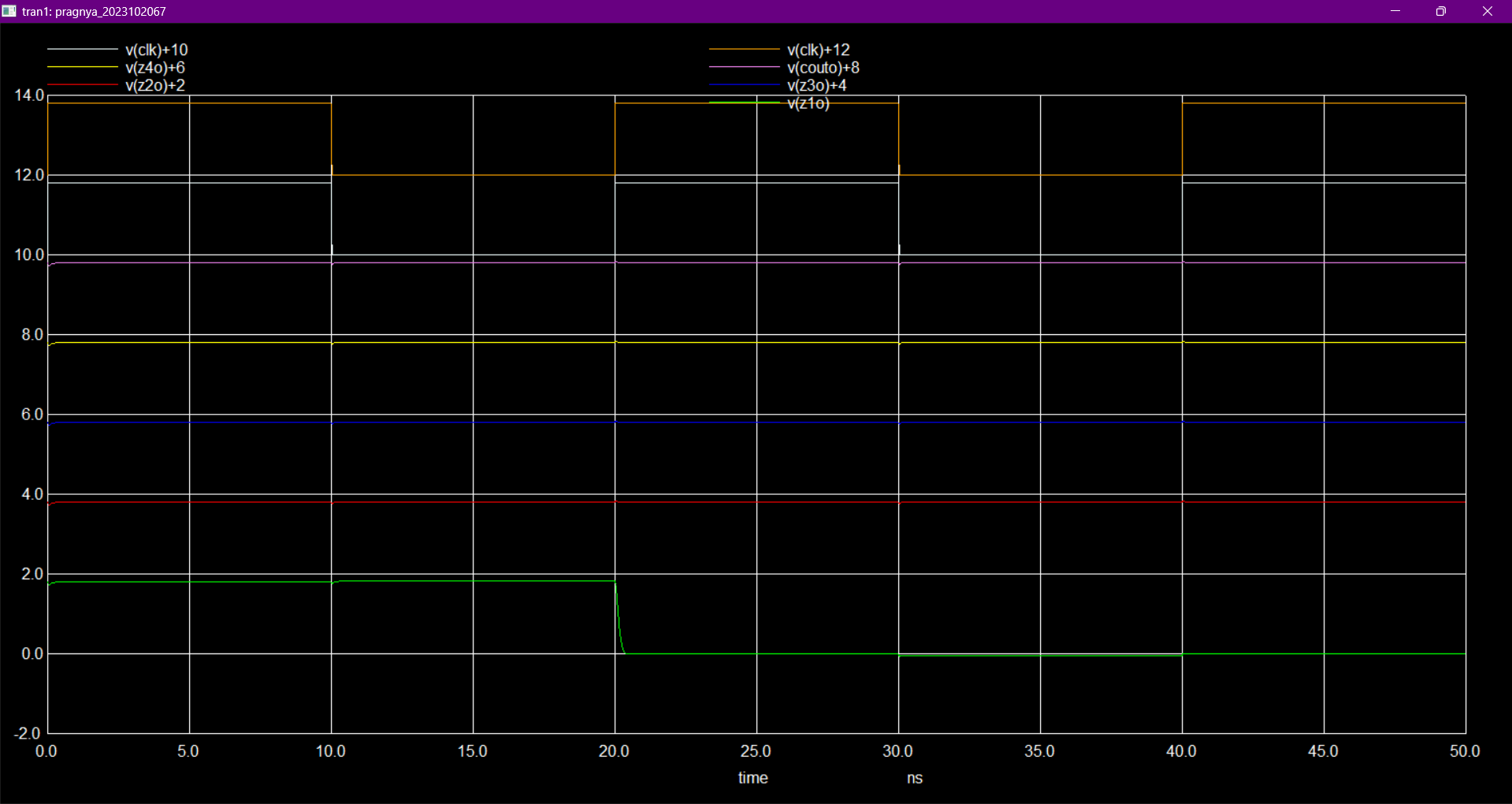
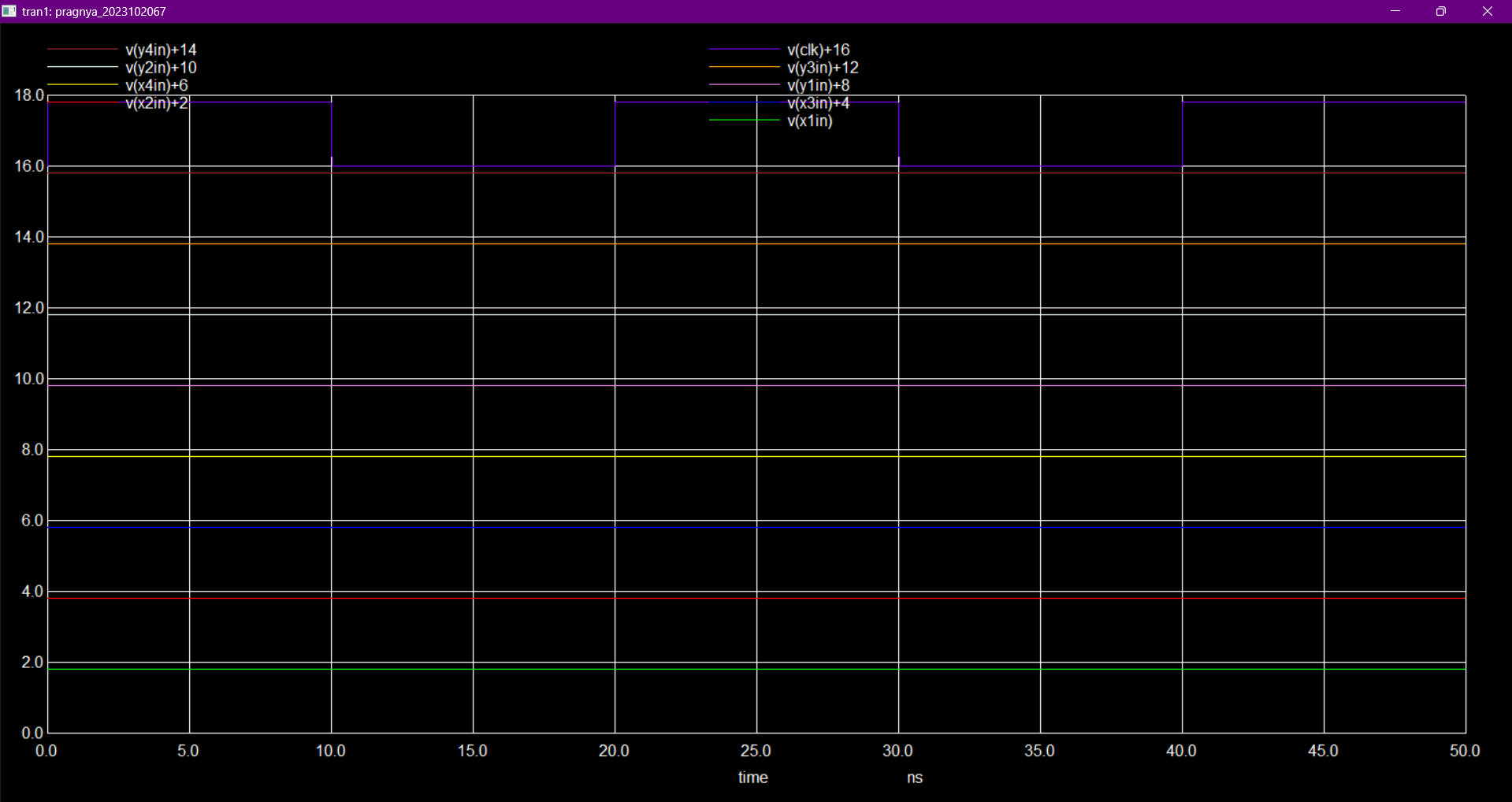
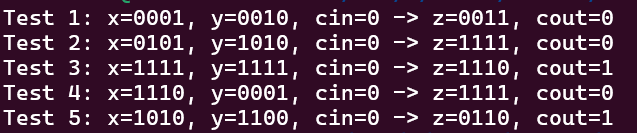
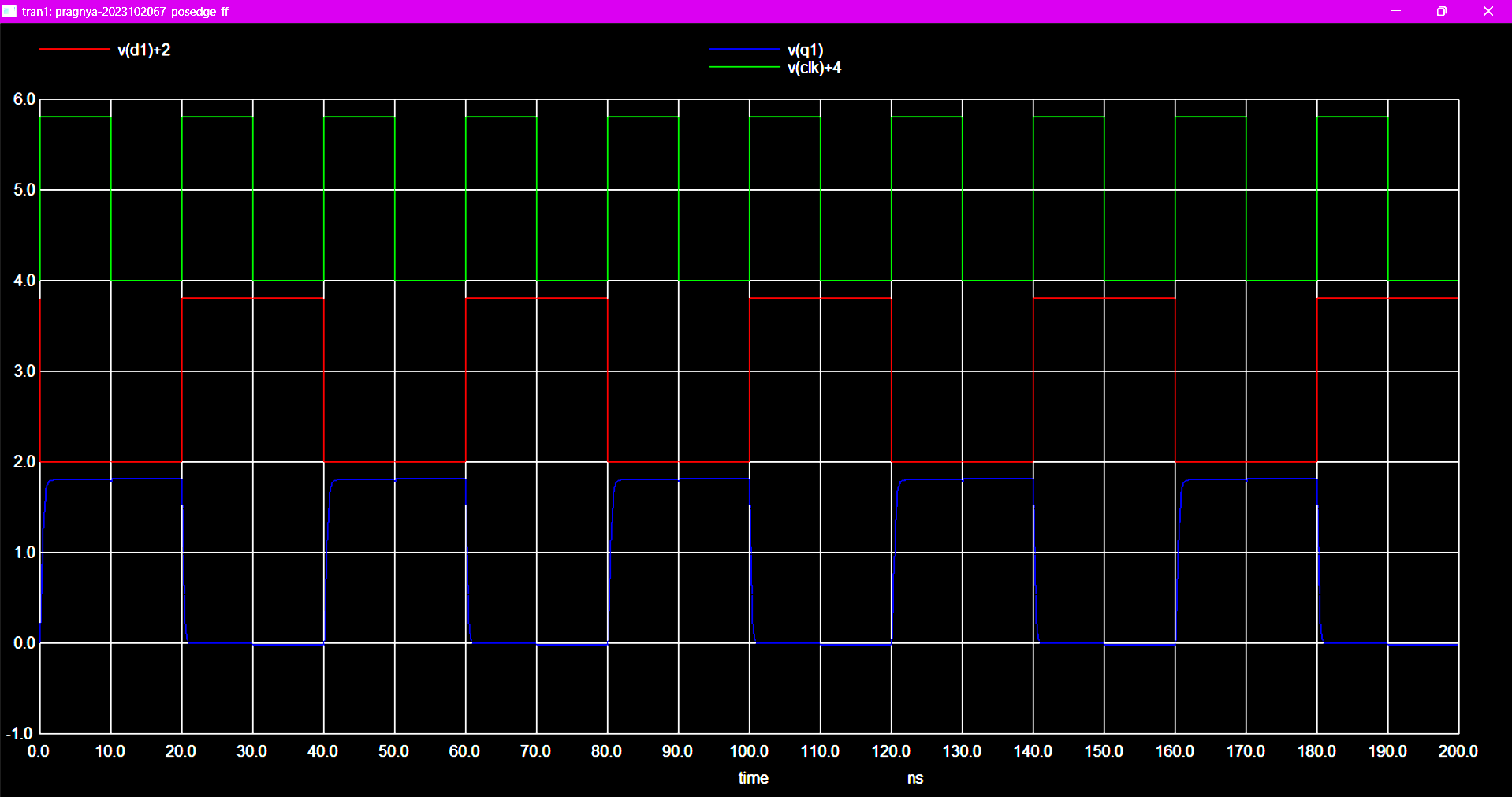
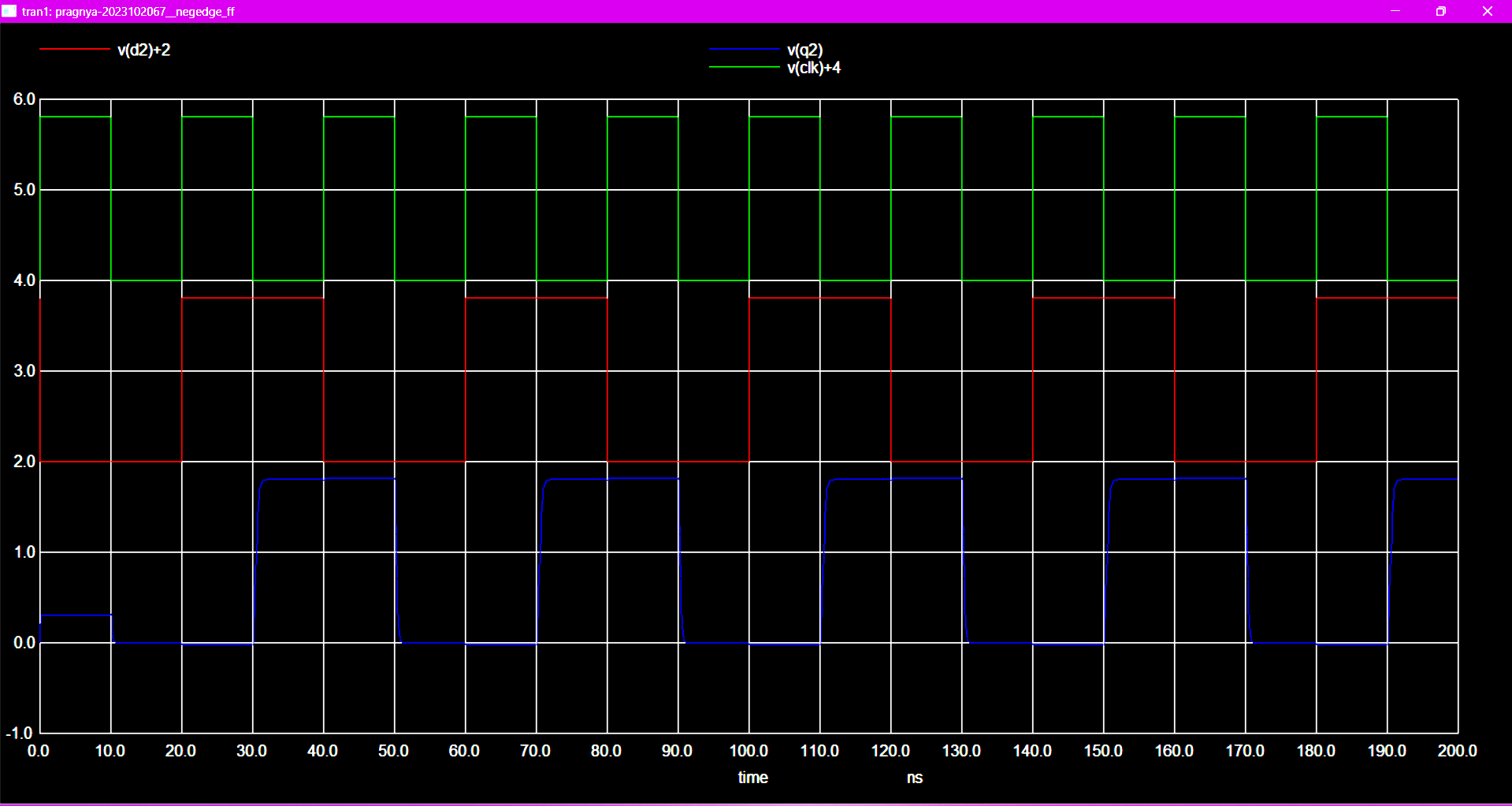
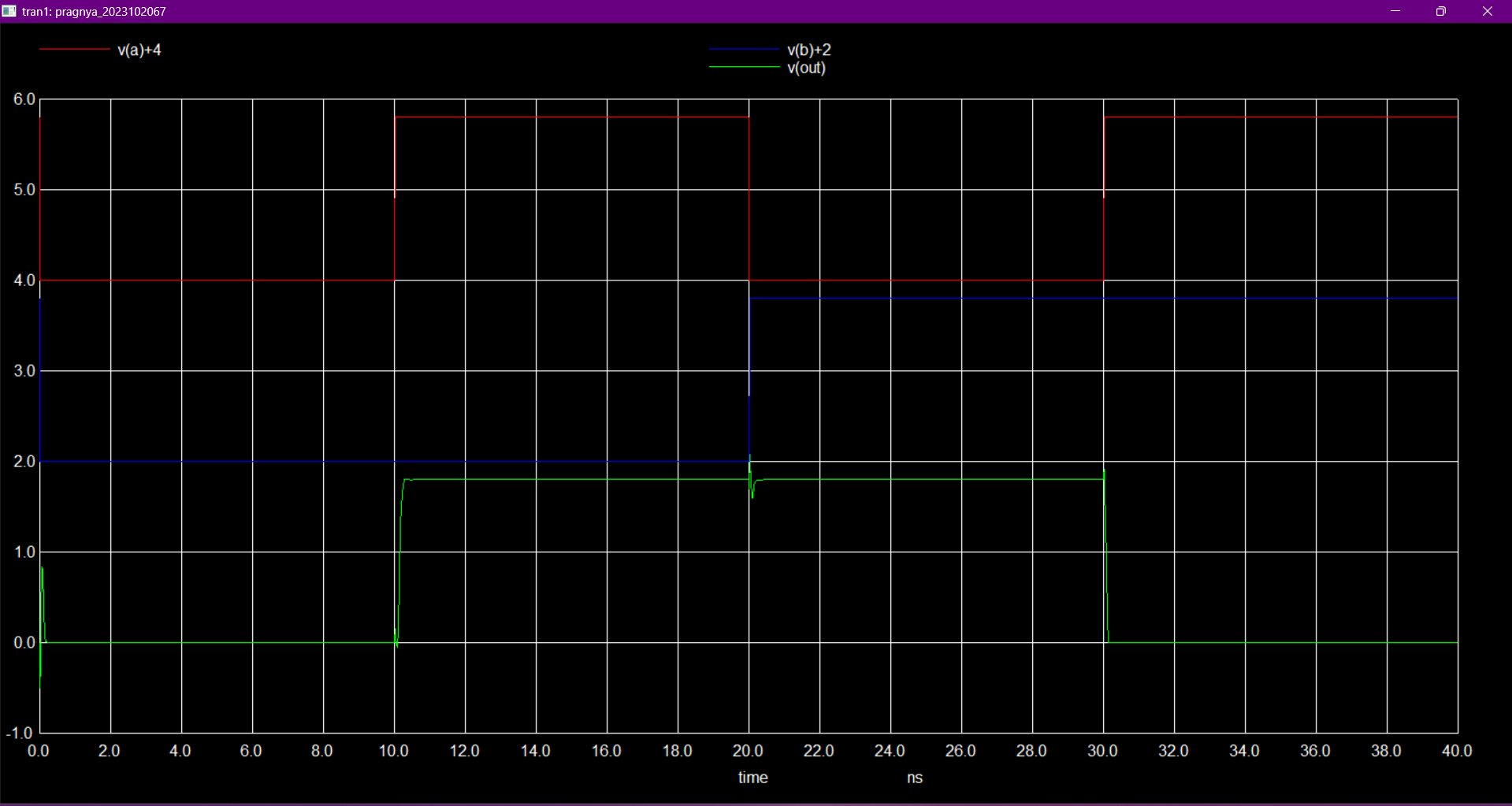
FINAL CLA  
OUTPUT when all inputs take high value  
we can see that at pos clk edge op is seen.

FINAL VERILOG OUTPUT

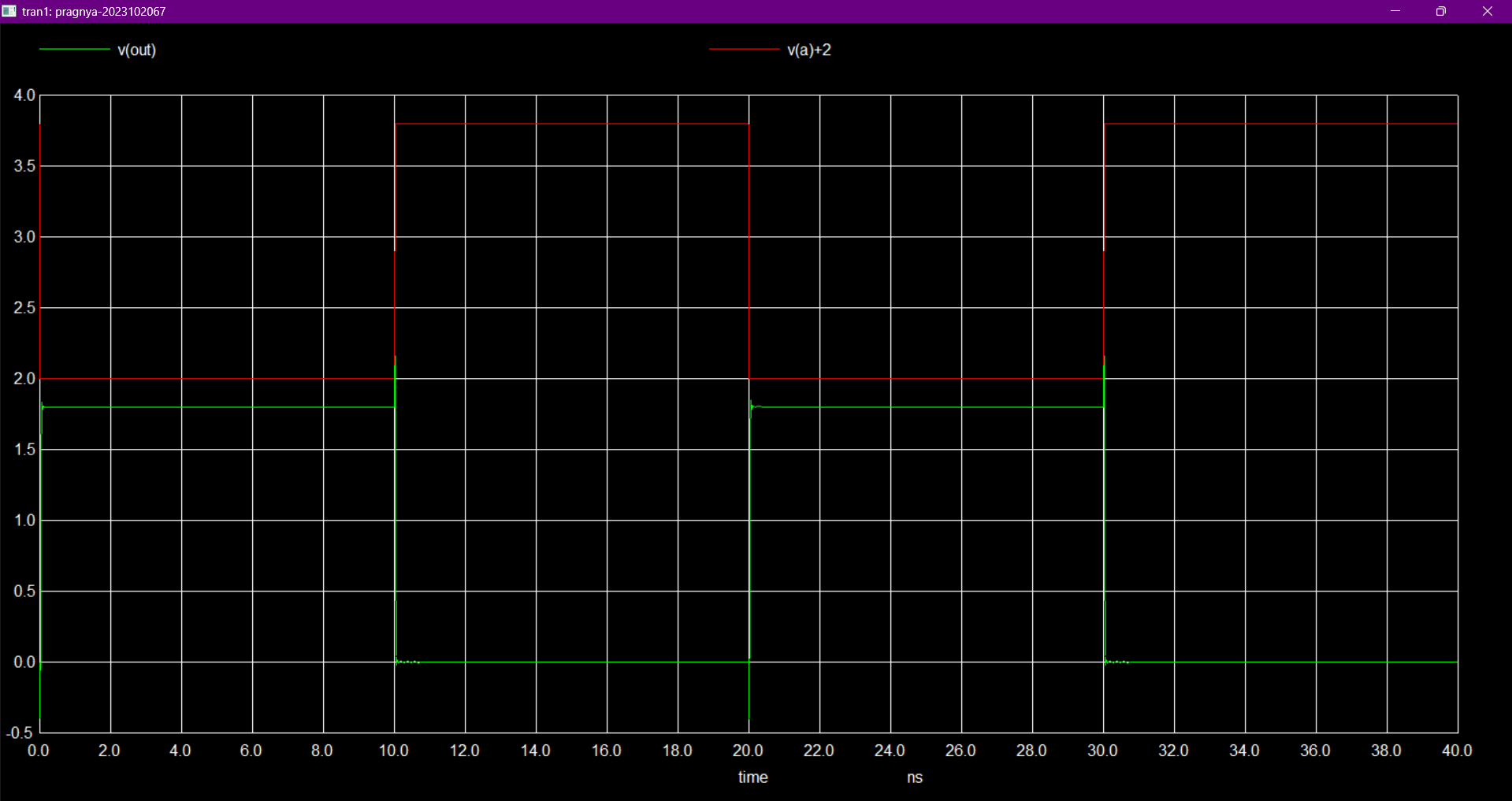
  
  
FINAL ANS- Cout, z[i]  
  
pos\_edge ff



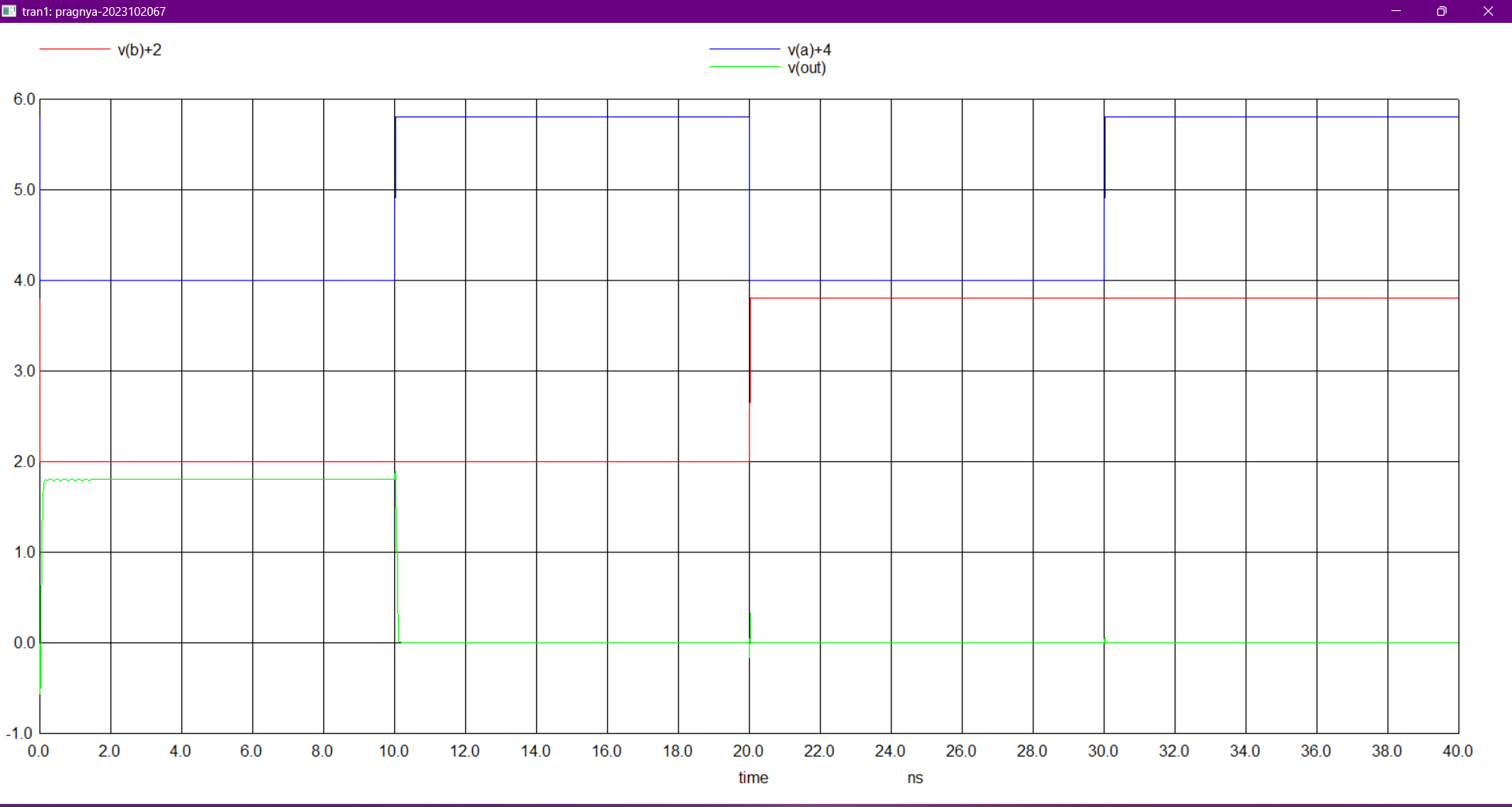
Neg\_edge ff

  
  
xor gate

Not gate



Nor gate

  
nand gate

